

AMENDMENT UNDER 37 C.F.R. § 1.116  
U.S. Appln. No.: 09/824,751  
Attorney Docket No.: Q63945

**REMARKS**

**I. Formal Matters**

Applicant thanks the Examiner for initialing the references listed on form PTO-1449 submitted with the Information Disclosure Statements filed on October 30, 2003.

**II. Claims**

Claims 1-7 and 9-13 are all the claims pending in this application. The Examiner has indicated that claim 8 has been allowed.

**A. Allowable Subject Matter**

The Examiner has rejected claims 1-5 and 11 under 35 U.S.C. § 112, second paragraph. Claims 1-5 and 11 have been amended to overcome the rejections under 35 U.S.C. § 112 by changing “outside of the device” to “outside of said semiconductor memory device.” The Examiner is respectfully requested to note these changes and should therefore withdraw the 35 U.S.C. § 112 rejection. Applicant respectfully requests that the Examiner acknowledge that claims 1-5 and 11 are now allowable as a result of the amendments.

**B. Rejections Under § 102.**

Claims 6, 7, 9, 10, 12, and 13 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Yamada et al. (U.S. Patent No. 6,091,655, hereinafter “Yamada”). Applicant traverses the rejections for the following reasons.

**Claims 6, 7, 9, 10, 12, and 13:** To be anticipated under 35 U.S.C. § 102, the reference must disclose every element of the Applicant’s claims. However, Yamada fails to disclose at least the following limitations of independent claim 6:

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“A signal hold circuit for taking and holding a data signal read out to the bit-line.” The signal hold circuit of the claimed invention takes and holds data signals read out to the bit line. There is no component in Yamada that holds a data signal. Yamada teaches data stored in the memory cell for holding only a reference signal level and then transmitted through a local probe to the read circuit (*see* col. 6, ln. 22-24, Yamada).

In Yamada, the information stored in the memory cells is fed through bit lines to a reference potential generation circuit which generates a reference potential (*see* col. 5, ln. 13-16, Yamada). By contrast, the invention as set forth in claim 6 recites a data signal that is read out to the bit line but is held in the signal hold circuit. Yamada does not teach a data signal but only a reference signal to be held in the memory cell (*see* col. 6, ln. 22-25, Yamada). In claim 6, the memory cell array and the signal hold circuit are different components.

Applicant respectfully submits that the Yamada reference fails to teach or suggest all of the claim limitations as set forth in independent claim 6. Therefore, independent claim 6 should be allowed. Additionally, since claims 7, 9, 12, and 13 depend from claim 6 and since the Yamada reference does not disclose all of the limitations of claim 6, Applicant submits that claims 7, 9, 12, and 13 are patentable at least by virtue of their dependency from claim 6. Claim 10 recites similar features. Therefore, Applicant submits that claim 10 should also be allowed. Accordingly, Applicant respectfully requests that the rejection of claims 6, 7, 9, 10, 12, and 13 under 35 U.S.C. § 102(e) be reconsidered and withdrawn.

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AMENDMENT UNDER 37 C.F.R. § 1.116

U.S. Appln. No.: 09/824,751

Attorney Docket No.: Q63945

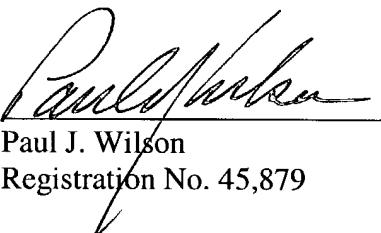
**III. Conclusion**

Claims 1-13 are all the claims pending in the application.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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